EC1201 DIGITAL ELECTRONICS 3 1 0 100

AIM

To learn the basic methods for the design of digital circuits and provide the fundamental concepts used in the design of digital systems

OBJECTIVES

- To introduce number systems and codes
- To introduce basic postulates of Boolean algebra and shows the correlation between Boolean expressions
- To introduce the methods for simplifying Boolean expressions
- To outline the formal procedures for the analysis and design of combinational circuits and sequential circuits
- To introduce the concept of memories and programmable logic devices.

UNIT I NUMBER SYSTEMS 9

Binary, Octal, Decimal, Hexadecimal-Number base conversions – complements – signed Binary numbers. Binary Arithmetic- Binary codes: Weighted –BCD-2421-Gray code-Excess 3 code-ASCII –Error detecting code – conversion from one code to another-Boolean postulates and laws –De-Morgan's Theorem- Principle of Duality- Boolean expression – Boolean function- Minimization of Boolean expressions – Sum of Products (SOP) –Product of Sums (POS)-Minterm- Maxterm- Canonical forms – Conversion between canonical forms –Karnaugh map Minimization – Don't care conditions.

UNIT II 9

LOGIC GATES: AND, OR, NOT, NAND, NOR, Exclusive – OR and Exclusive – NOR- Implementations of Logic Functions using gates, NAND –NOR implementations –Multi level gate implementations- Multi output gate implementations. TTL and CMOS Logic and their characteristics –Tristate gates.

COMBINATIONAL CIRCUITS:

Design procedure – Adders-Subtractors – Serial adder/ Subtractor - Parallel adder/ Subtractor- Carry look ahead adder- BCD adder- Magnitude Comparator- Multiplexer/ Demultiplexer- encoder / decoder – parity checker – code converters. Implementation of combinational logic using MUX, ROM, PAL and PLA.

UNIT III SEQUENTIAL CIRCUIT 9

Flip flops SR, JK, T, D and Master slave – Characteristic table and equation –Application table – Edge triggering –Level Triggering –Realization of one flip flop using other flip flops –Asynchronous / Ripple counters – Synchronous counters –Modulo – n counter –Classification of sequential circuits – Moore and Mealy -Design of Synchronous counters: state diagram- State table –State minimization –State assignment- ASM-Excitation table and maps-Circuit implementation - Register – shift registers- Universal shift register – Shift counters – Ring counters.

UNIT IV ASYNCHRONOUS SEQUENTIAL CIRCUITS 9

Design of fundamental mode and pulse mode circuits – primitive state / flow table – Minimization of primitive state table –state assignment – Excitation table – Excitation map- cycles – Races –Hazards: Static –Dynamic –Essential –Hazards elimination.

UNIT V MEMORY DEVICES 9

Classification of memories –RAM organization – Write operation –Read operation – Memory cycle - Timing wave forms – Memory decoding – memory expansion – Static RAM Cell-Bipolar RAM cell – MOSFET RAM cell –Dynamic RAM cell –ROM organization - PROM –EPROM – EEPROM –EAPROM –Programmable Logic Devices –Programmable Logic Array (PLA)- Programmable Array Logic (PAL)-Field Programmable Gate Arrays (FPGA).

TUTORIAL 15
TOTAL : 60

1. M. Morris Mano, Digital Design, 3.ed., Prentice Hall of India Pvt. Ltd., New Delhi, 2003/Pearson Education (Singapore) Pvt. Ltd., New Delhi, 2003 – (Unit I, II, V)
2. John .M Yarbrough, Digital Logic Applications and Design, Thomson- Vikas publishing house, New Delhi, 2002. (Unit III, IV)

REFERENCES

1. S. Salivahanan and S. Arivazhagan, Digital Circuits and Design, 2nd ed., Vikas Publishing House Pvt. Ltd, New Delhi, 2004
2. Charles H.Roth. "Fundamentals of Logic Design", Thomson Publication Company, 2003.
3. Donald P.Leach and Albert Paul Malvino, Digital Principles and Applications, 5 ed., Tata McGraw Hill Publishing Company Limited, New Delhi, 2003.
4. R.P.Jain, Modern Digital Electronics, 3 ed., Tata McGraw–Hill publishing company limited, New Delhi, 2003.
5. Thomas L. Floyd, Digital Fundamentals, Pearson Education, Inc, New Delhi, 2003
6. Donald D.Givone, Digital Principles and Design, Tata Mc-Graw-Hill Publishing company limited, New Delhi, 2003.